FIG. 1

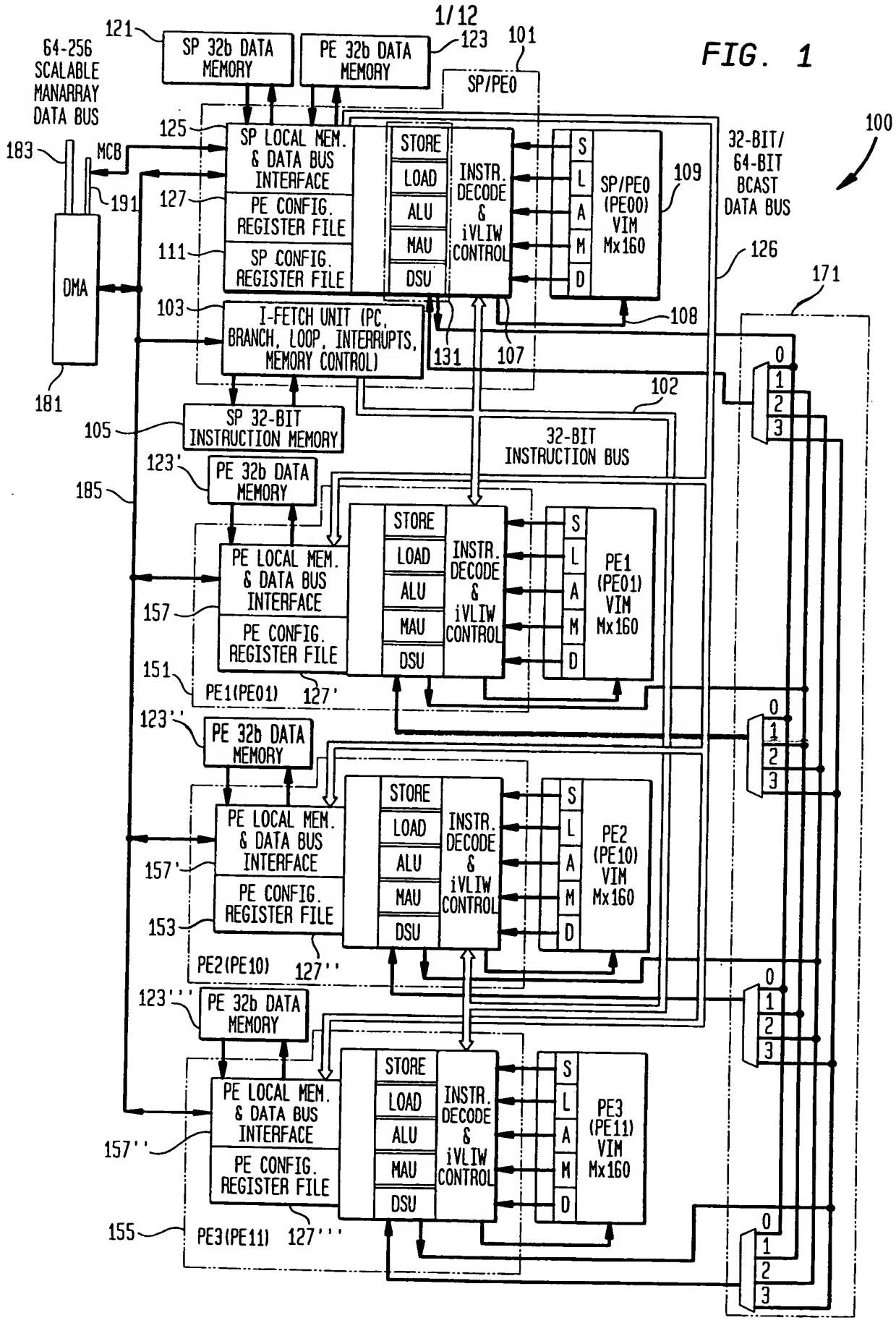

64-256 SCALABLE MANARRAY DATA BUS
121
SP 32b DATA MEMORY
PE 32b DATA MEMORY
123
101
SP/PE0
100
32-BIT/ 64-BIT BCAST DATA BUS
183
MCB
191
125
SP LOCAL MEM. & DATA BUS INTERFACE
127
PE CONFIG. REGISTER FILE
111
SP CONFIG. REGISTER FILE
STORE
LOAD
ALU
MAU
DSU
INSTR. DECODE & iVLIW CONTROL
S
L
A
M
D
SP/PE0 (PE00) VIM Mx160
109
126
171
OMA
181
103
I-FETCH UNIT (PC, BRANCH, LOOP, INTERRUPTS, MEMORY CONTROL)
131
107
108
102
105
SP 32-BIT INSTRUCTION MEMORY
32-BIT INSTRUCTION BUS
123'
185
PE 32b DATA MEMORY
PE LOCAL MEM. & DATA BUS INTERFACE
157
PE CONFIG. REGISTER FILE
PE1 (PE01) VIM Mx160
151
PE1(PE01)
127'
123''
PE 32b DATA MEMORY
157'
153
PE2 (PE10) VIM Mx160
PE2(PE10)
127''
123'''
PE 32b DATA MEMORY
157''
PE3 (PE11) VIM Mx160
155
PE3(PE11)
127'''
0
1
2
3

FIG. 2

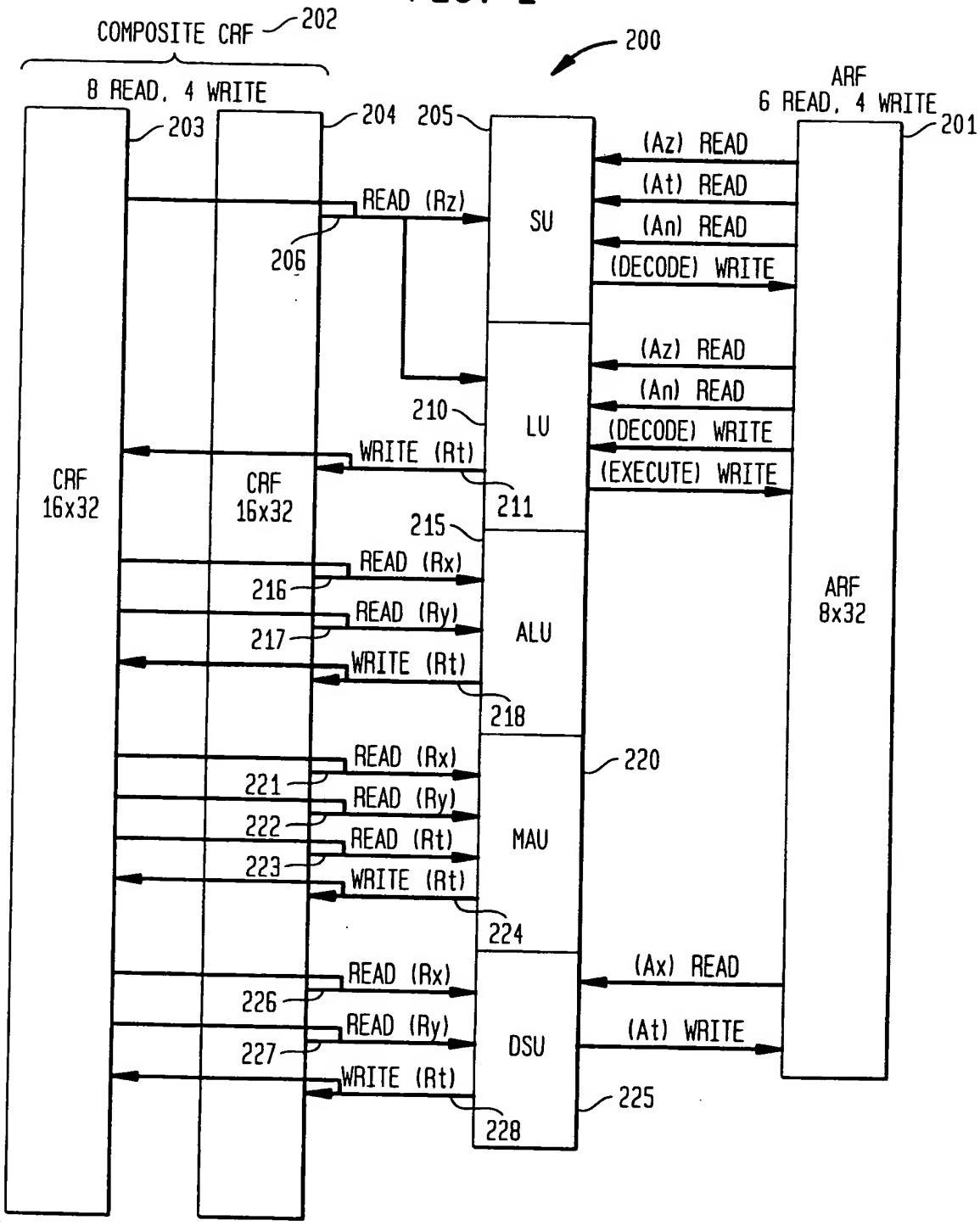

COMPOSITE CRF
202
8 READ, 4 WRITE
200
ARF
6 READ, 4 WRITE
201
203
204
205
CRF
16x32
CRF
16x32
READ (Rz)
206
SU
(Az) READ
(At) READ
(An) READ
(DECODE) WRITE
(Az) READ
(An) READ
(DECODE) WRITE
(EXECUTE) WRITE
210
LU
WRITE (Rt)
211
215
READ (Rx)
216
READ (Ry)
217
ALU
WRITE (Rt)
218
ARF
8x32
READ (Rx)
221
READ (Ry)
222
READ (Rt)
223
MAU
WRITE (Rt)
224
220
READ (Rx)
226
READ (Ry)
227
DSU
WRITE (Rt)
228
(Ax) READ
(At) WRITE
225

FIG. 3

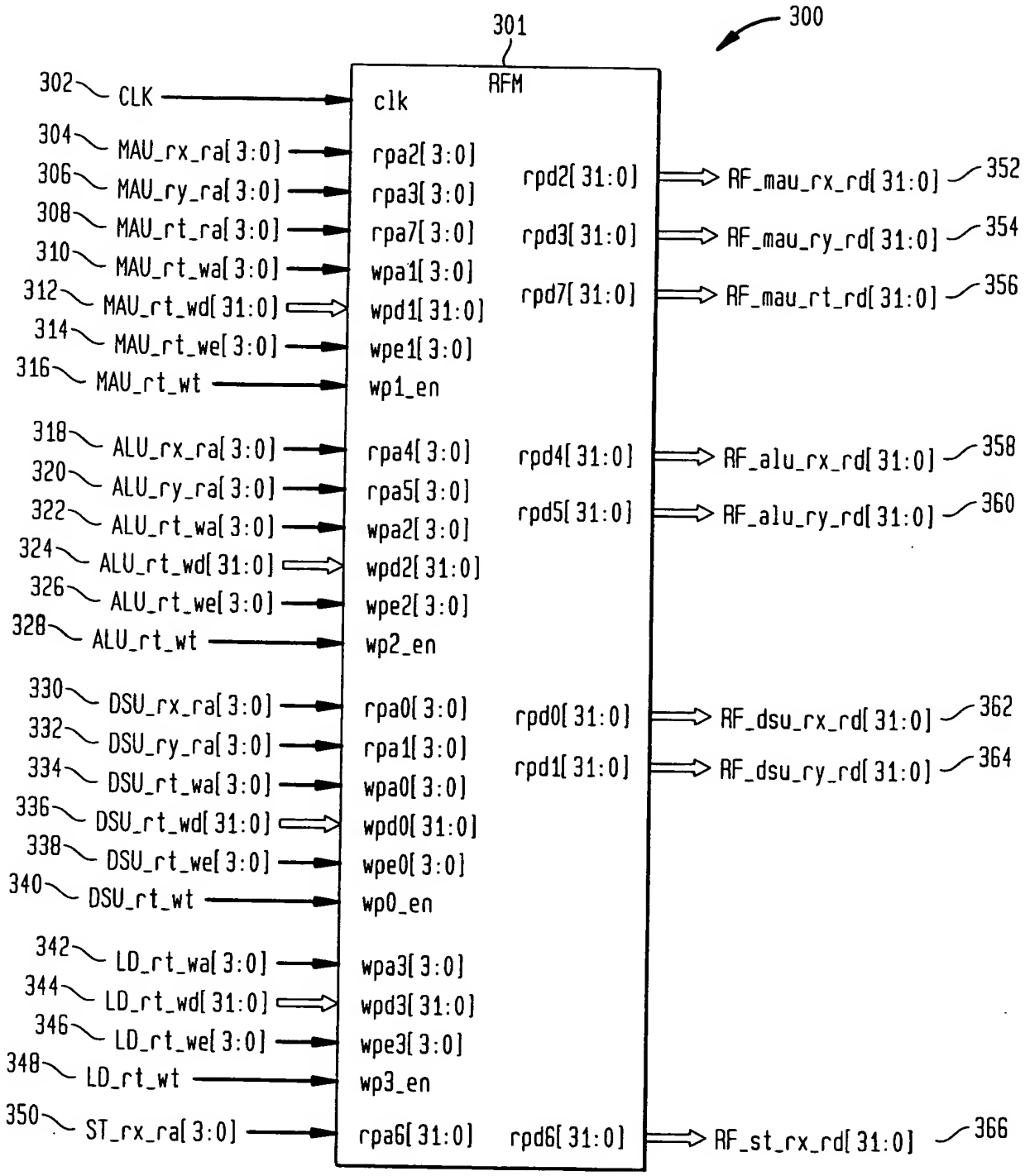

300
301
RFM
clk
302 CLK
304 MAU_rx_ra[3:0]
306 MAU_ry_ra[3:0]
308 MAU_rt_ra[3:0]
310 MAU_rt_wa[3:0]
312 MAU_rt_wd[31:0]
314 MAU_rt_we[3:0]
316 MAU_rt_wt
318 ALU_rx_ra[3:0]
320 ALU_ry_ra[3:0]
322 ALU_rt_wa[3:0]
324 ALU_rt_wd[31:0]
326 ALU_rt_we[3:0]
328 ALU_rt_wt
330 DSU_rx_ra[3:0]
332 DSU_ry_ra[3:0]
334 DSU_rt_wa[3:0]
336 DSU_rt_wd[31:0]
338 DSU_rt_we[3:0]
340 DSU_rt_wt
342 LD_rt_wa[3:0]
344 LD_rt_wd[31:0]
346 LD_rt_we[3:0]
348 LD_rt_wt
350 ST_rx_ra[3:0]
rpa2[3:0]
rpa3[3:0]
rpa7[3:0]
wpa1[3:0]
wpd1[31:0]
wpe1[3:0]
wp1_en
rpa4[3:0]
rpa5[3:0]
wpa2[3:0]
wpd2[31:0]
wpe2[3:0]
wp2_en
rpa0[3:0]
rpa1[3:0]
wpa0[3:0]
wpd0[31:0]
wpe0[3:0]
wp0_en
wpa3[3:0]
wpd3[31:0]
wpe3[3:0]
wp3_en
rpa6[31:0]
rpd2[31:0] RF_mau_rx_rd[31:0] 352
rpd3[31:0] RF_mau_ry_rd[31:0] 354
rpd7[31:0] RF_mau_rt_rd[31:0] 356
rpd4[31:0] RF_alu_rx_rd[31:0] 358
rpd5[31:0] RF_alu_ry_rd[31:0] 360
rpd0[31:0] RF_dsu_rx_rd[31:0] 362
rpd1[31:0] RF_dsu_ry_rd[31:0] 364
rpd6[31:0] RF_st_rx_rd[31:0] 366

FIG. 4A

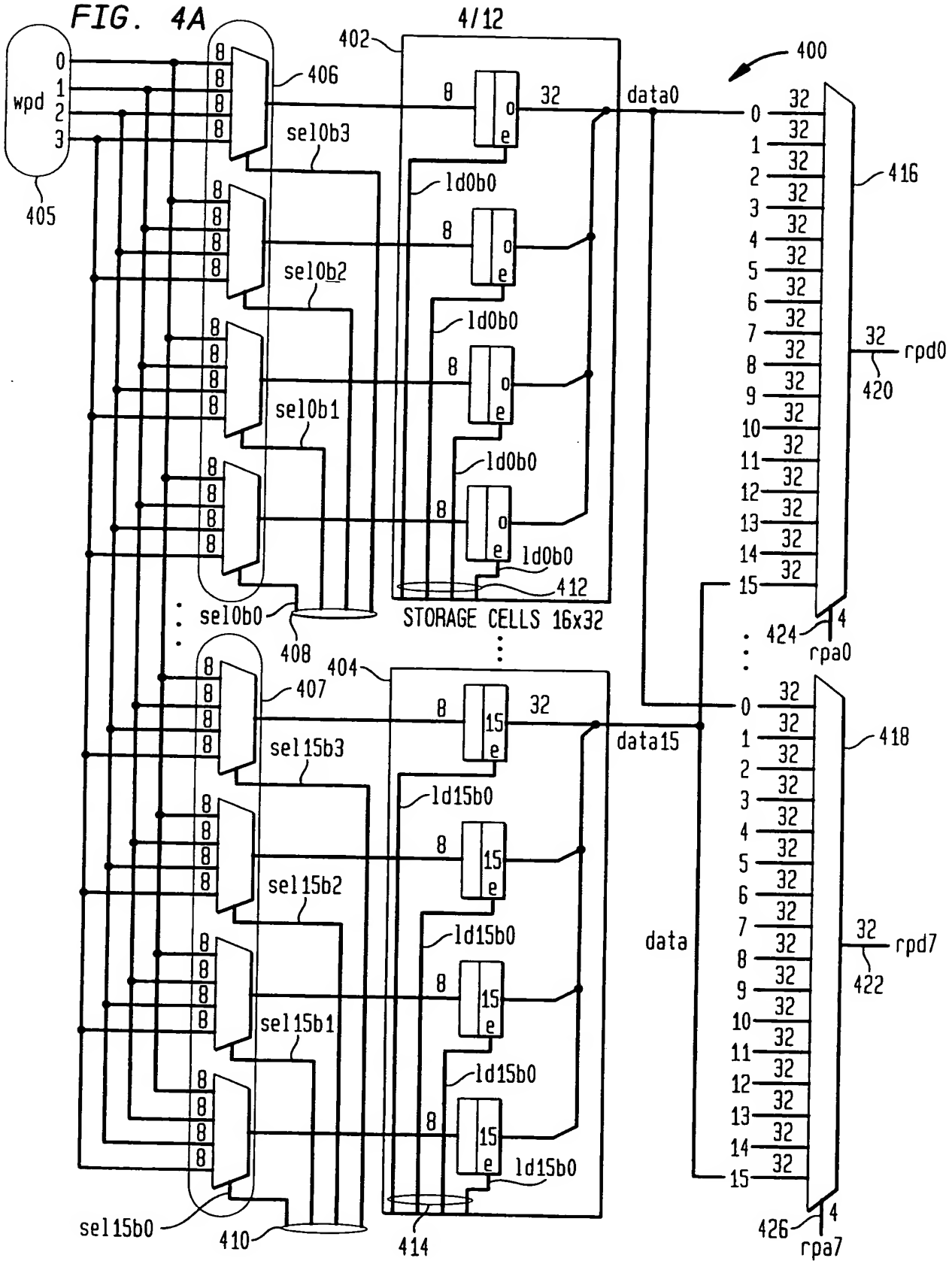

wpd
0
1
2
3
405
406
407
sel0b3
sel0b2
sel0b1
sel0b0
408
sel15b3
sel15b2
sel15b1
sel15b0
410
402
404
412
414
STORAGE CELLS 16x32
ld0b0
ld15b0
8
32
o
e
15
data0
data15
data
400
416
418
420
422
424
426
rpd0
rpd7
rpa0
rpa7
4

FIG. 4B

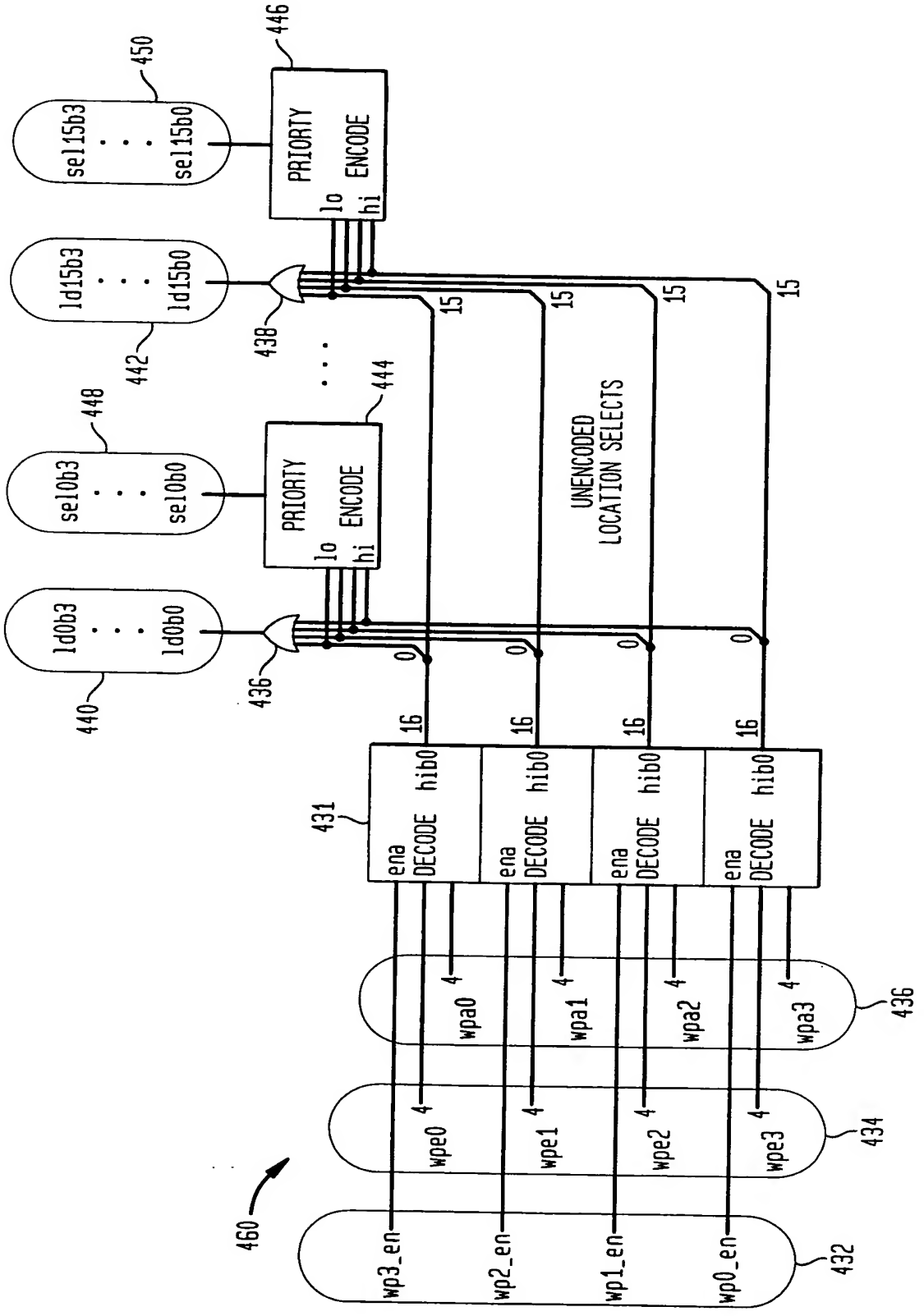

sel15b3
sel15b0
450
PRIORITY ENCODE
lo
hi
446
ld15b3
ld15b0
442
438
sel0b3
sel0b0
448
PRIORITY ENCODE
444
ld0b3
ld0b0
440
436
UNENCODED LOCATION SELECTS
15
0
16
431
ena DECODE hib0
wpa0
wpa1
wpa2
wpa3
436
wpe0
wpe1
wpe2
wpe3
434
wp3_en
wp2_en
wp1_en
wp0_en
432
460

FIG. 4C

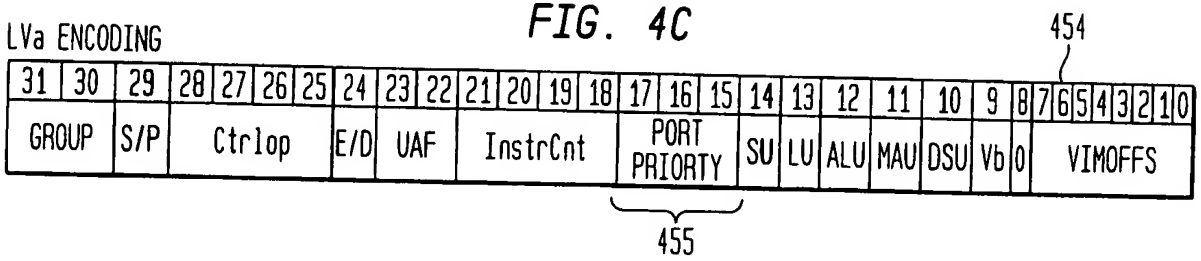


FIG. 4D

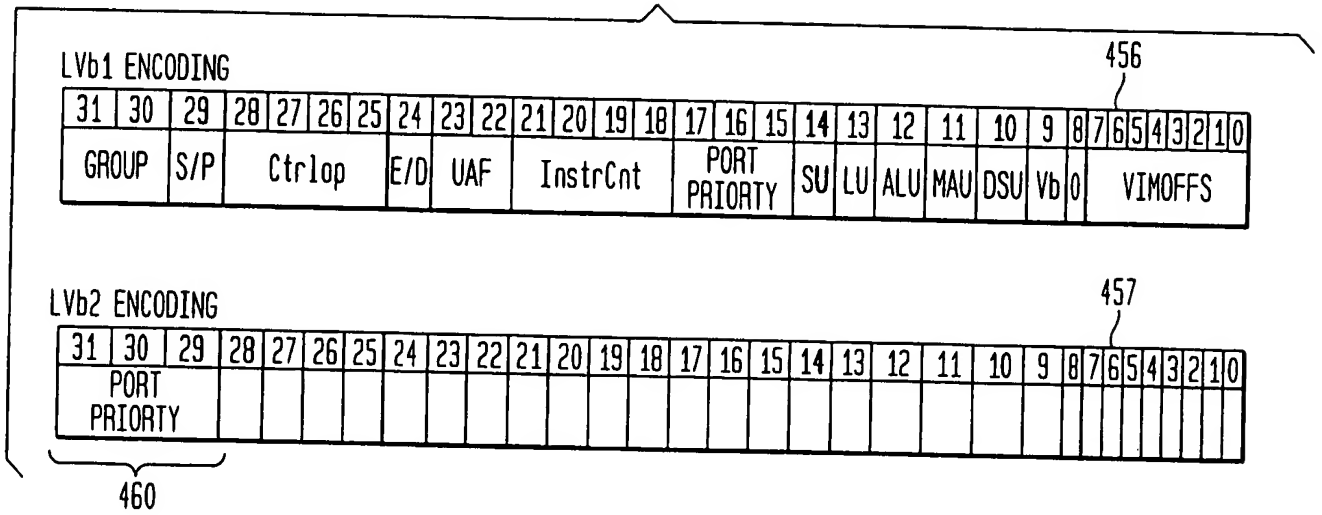


FIG. 4E

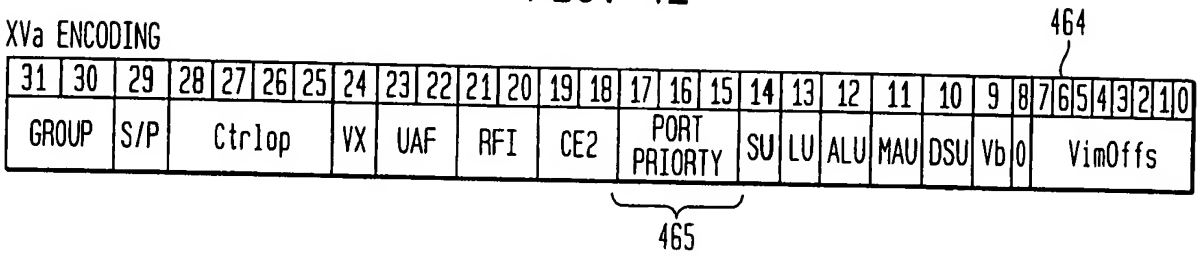


FIG. 4F

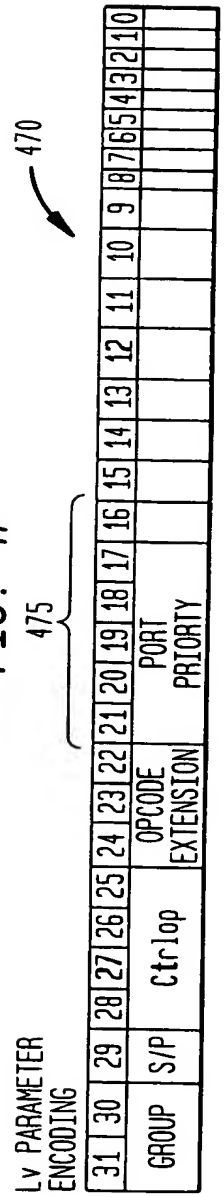

Lv PARAMETER ENCODING
470
475
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
GROUP
S/P
Ctrlop
OPCODE EXTENSION
PORT PRIORITY

FIG. 5

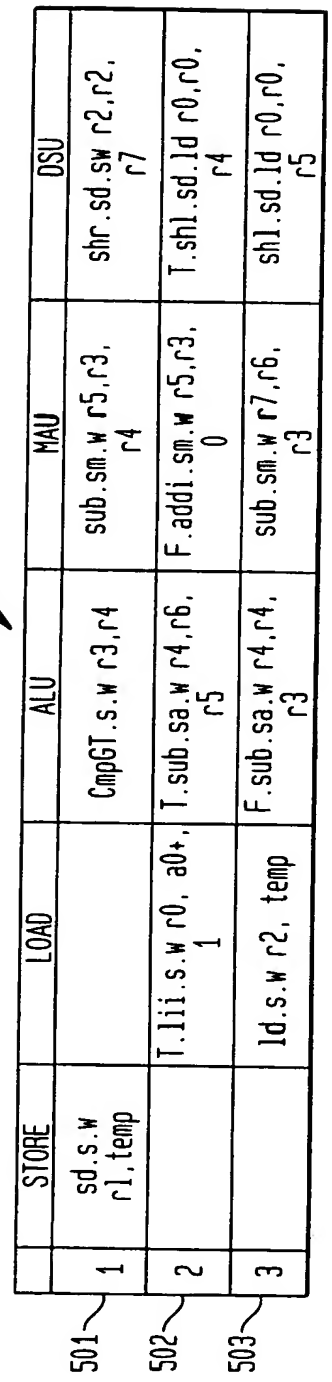

500
STORE
LOAD
ALU
MAU
DSU
1
sd.s.w r1, temp
CmpGT.s.w r3,r4
sub.sm.w r5,r3, r4
shr.sd.sw r2,r2, r7
2
T.lii.s.w r0, a0+, 1
T.sub.sa.w r4,r6, r5
F.addi.sm.w r5,r3, 0
T.shl.sd.ld r0,r0, r4
3
ld.s.w r2, temp
F.sub.sa.w r4,r4, r3
sub.sm.w r7,r6, r3
shl.sd.ld r0,r0, r5
501
502
503

FIG. 6

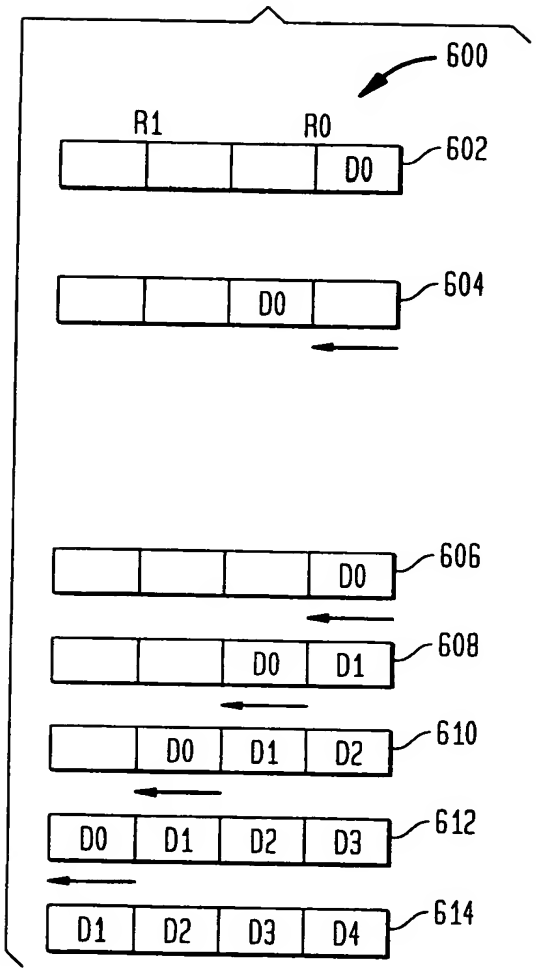

600
R1
R0
D0
602
D0
604
D0
606
D0
D1
608
D0
D1
D2
610
D0
D1
D2
D3
612
D1
D2
D3
D4
614

FIG. 7

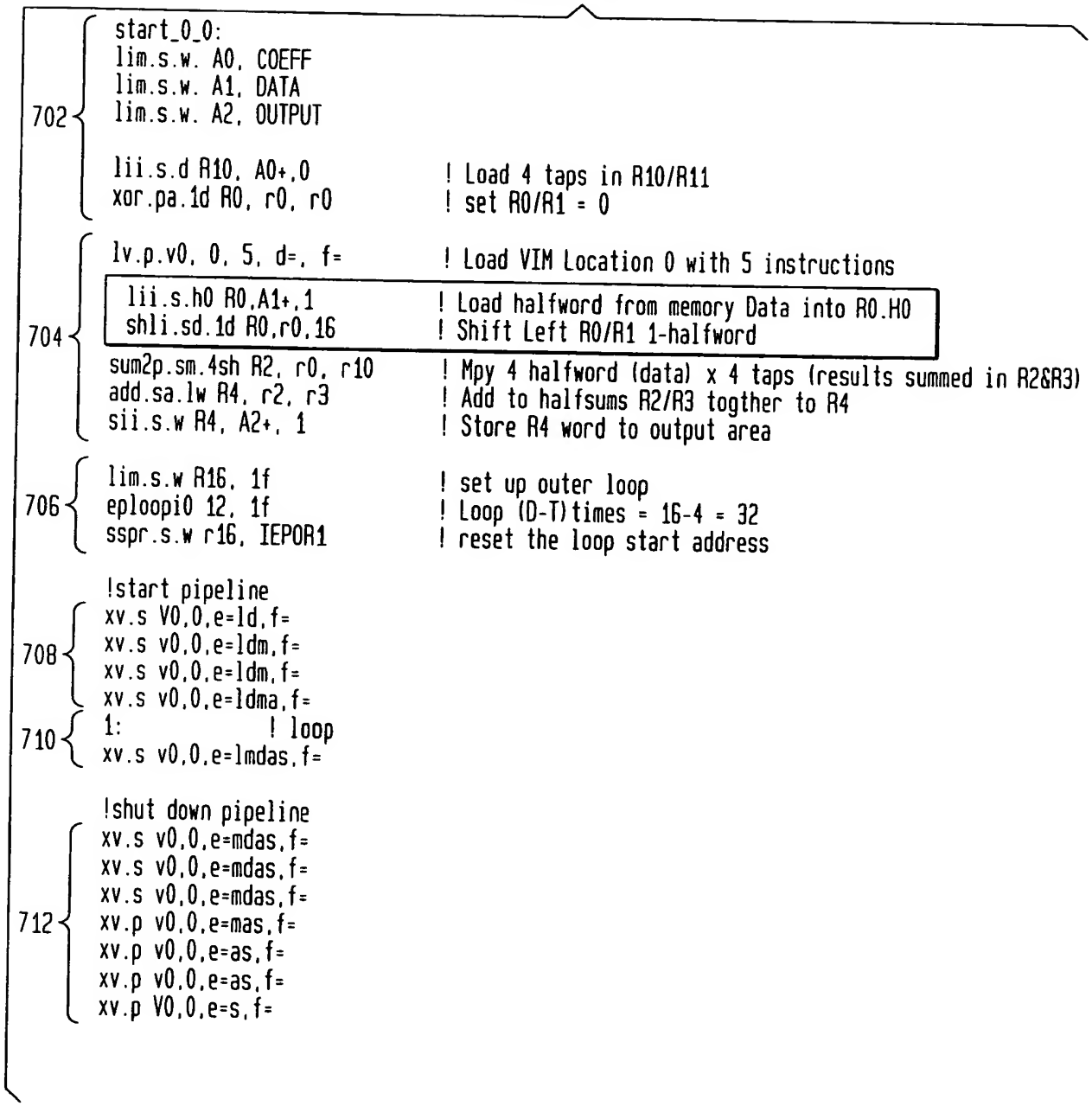

start_0_0:
lim.s.w. A0, COEFF
lim.s.w. A1, DATA
lim.s.w. A2, OUTPUT
702
lii.s.d R10, A0+,0 ! Load 4 taps in R10/R11
xor.pa.1d R0, r0, r0 ! set R0/R1 = 0
lv.p.v0, 0, 5, d=, f= ! Load VIM Location 0 with 5 instructions
lii.s.h0 R0,A1+,1 ! Load halfword from memory Data into R0.H0
shli.sd.1d R0,r0,16 ! Shift Left R0/R1 1-halfword
704
sum2p.sm.4sh R2, r0, r10 ! Mpy 4 halfword (data) x 4 taps (results summed in R2&R3)
add.sa.lw R4, r2, r3 ! Add to halfsums R2/R3 togther to R4
sii.s.w R4, A2+, 1 ! Store R4 word to output area
lim.s.w R16, 1f ! set up outer loop
706
eploopi0 12, 1f ! Loop (D-T) times = 16-4 = 32
sspr.s.w r16, IEPOR1 ! reset the loop start address
!start pipeline
xv.s V0,0,e=ld,f=
708
xv.s v0,0,e=ldm,f=
xv.s v0,0,e=ldm,f=
xv.s v0,0,e=ldma,f=
1: ! loop
710
xv.s v0,0,e=lmdas,f=
!shut down pipeline
xv.s v0,0,e=mdas,f=
xv.s v0,0,e=mdas,f=
xv.s v0,0,e=mdas,f=
712
xv.p v0,0,e=mas,f=
xv.p v0,0,e=as,f=
xv.p v0,0,e=as,f=
xv.p V0,0,e=s,f=

FIG. 8

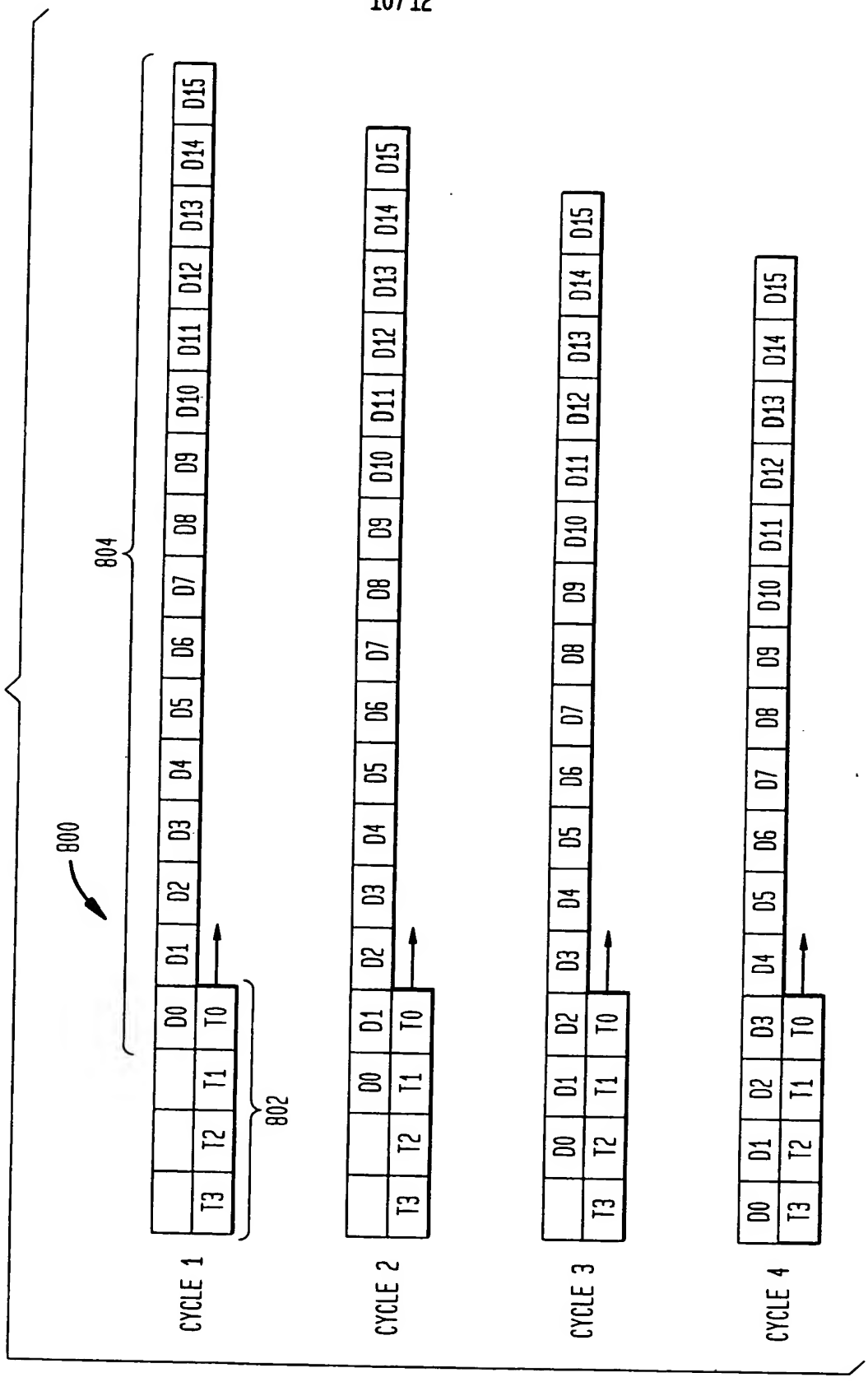

800
804
802
CYCLE 1
CYCLE 2
CYCLE 3
CYCLE 4
T3
T2
T1
T0
D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15

FIG. 9

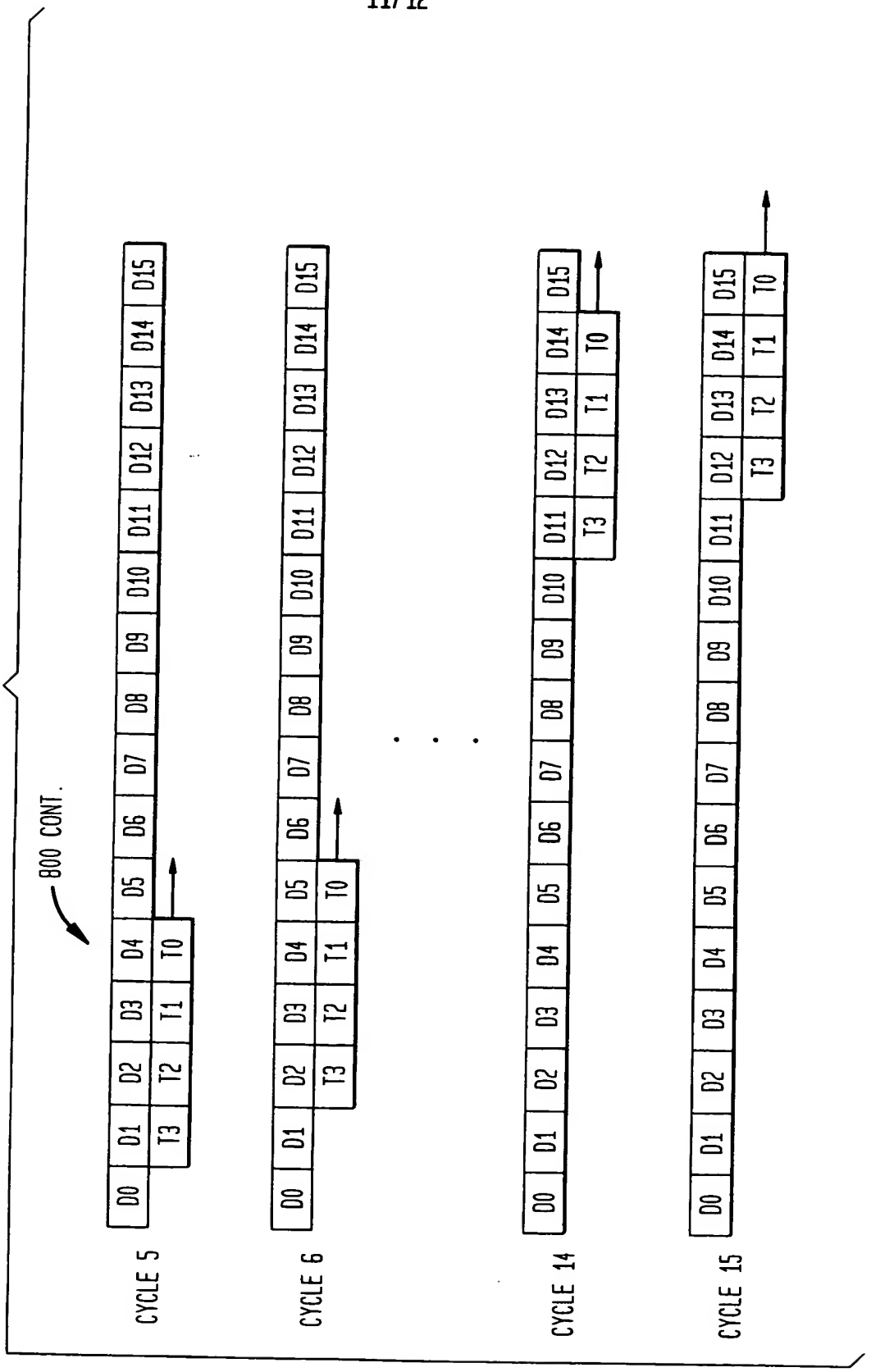
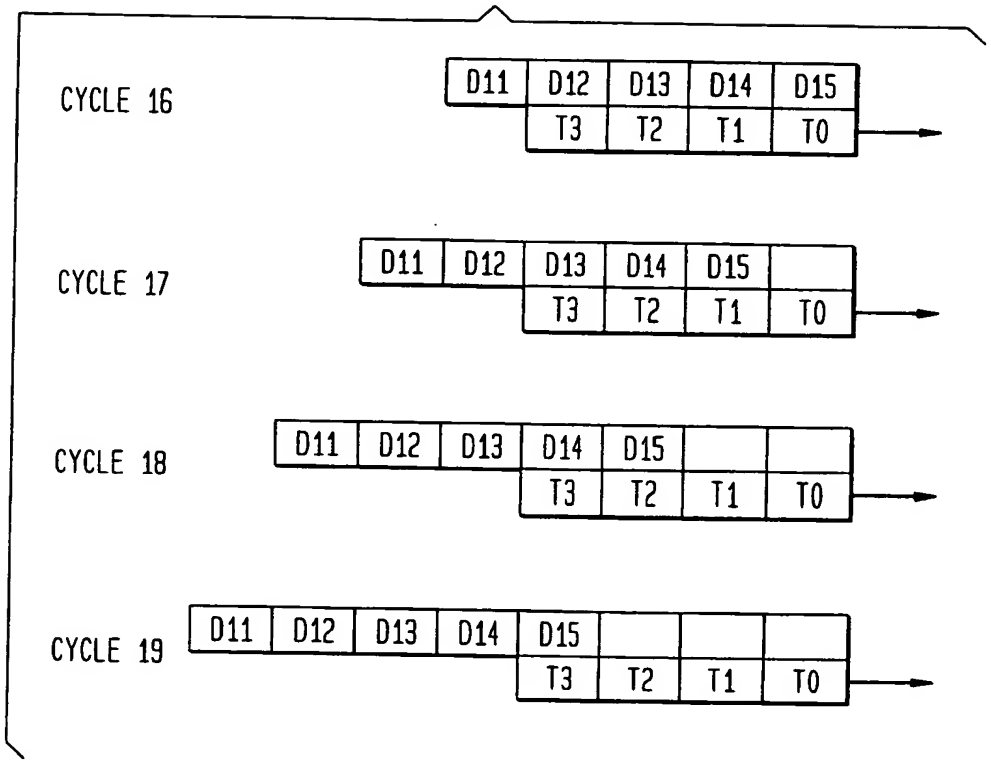

800 CONT.
CYCLE 5
CYCLE 6
CYCLE 14
CYCLE 15
D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15
T3 T2 T1 T0

FIG. 10


CYCLE 16
D11 D12 D13 D14 D15
T3 T2 T1 T0
CYCLE 17
D11 D12 D13 D14 D15
T3 T2 T1 T0
CYCLE 18
D11 D12 D13 D14 D15
T3 T2 T1 T0
CYCLE 19
D11 D12 D13 D14 D15
T3 T2 T1 T0